



Architecture of High Performance Computers: Volume I: Uniprocessors and Vector Processors (Computer Science) (Vol 1)

Roland N. Ibbett

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This revised, updated and expanded text deals mainly with techniques used in uniprocessor architectures to attain high performance. Many of these techniques involve some form of parallelism, which is hidden from the user. Developments in the Cray and Cyber 205 architectures are detailed and new material is included on array architectures, using the DAP as a case study and on multiprocessor architectures using C.mmp, the butterfly and the transputer as examples. The material is designed to accompany undergraduate courses in computer architecture and constitute a core of material presented in third and fourth year courses in the Computer Science Department at Edinburgh University.

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